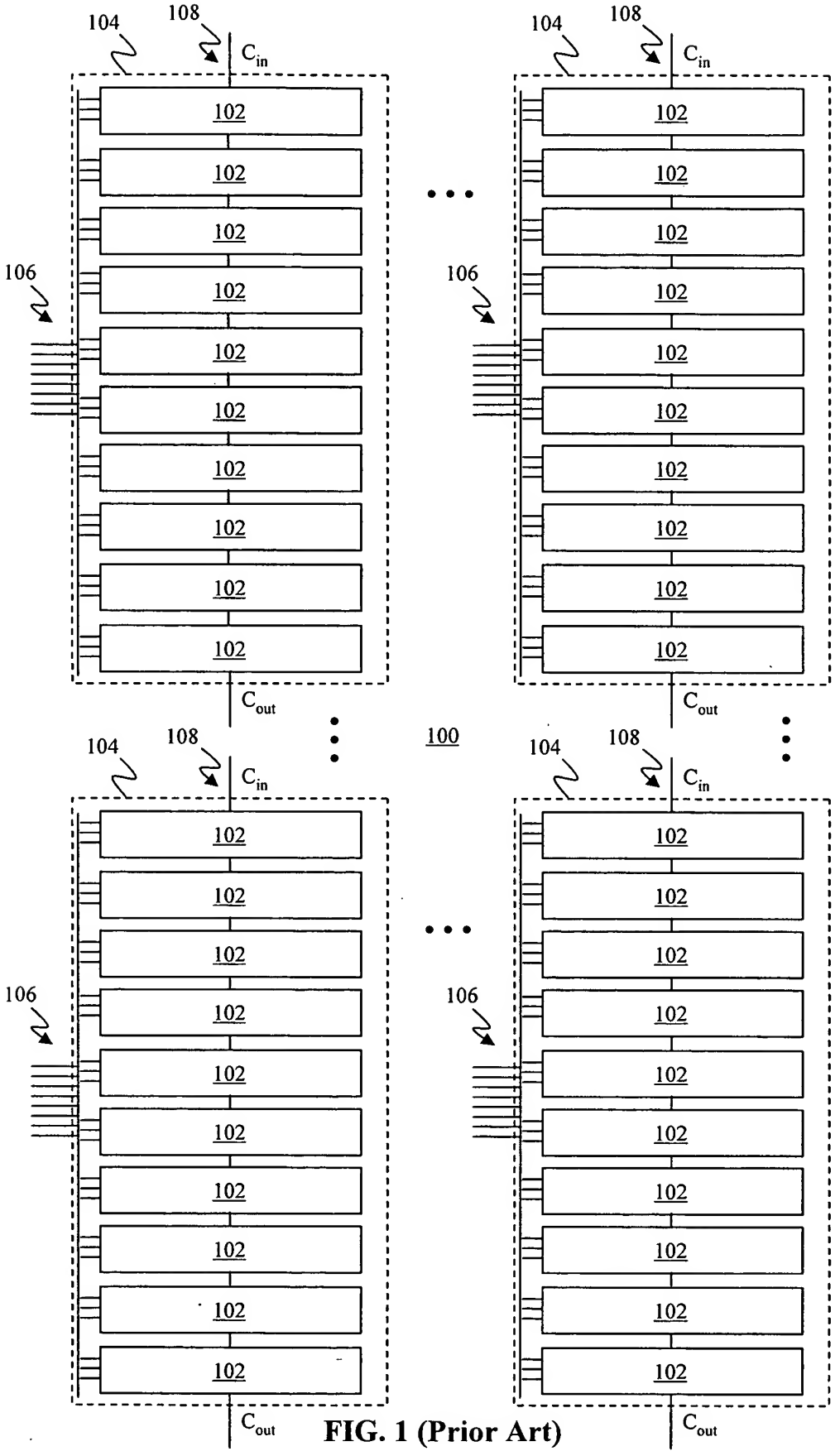

FIG. 1 (Prior Art)

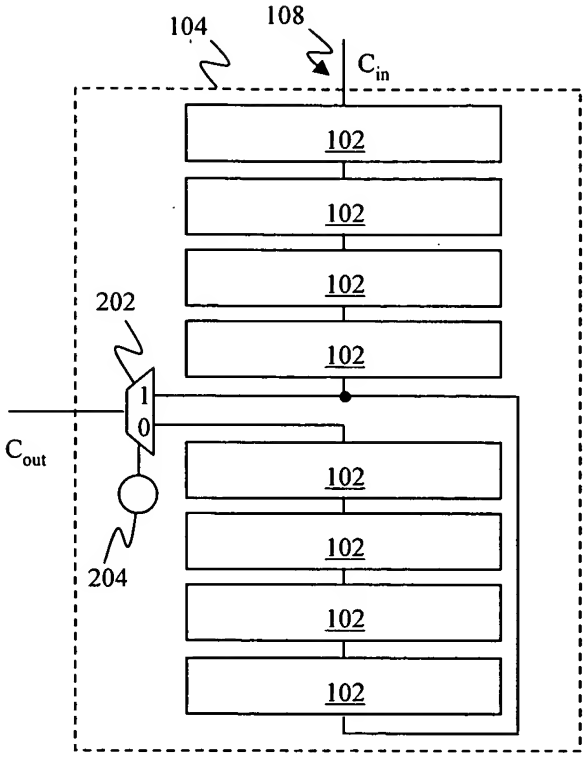
104
108
C_{in}
102
102
102
102
202
1
0
C_{out}
102
102
102
102
204

FIG. 2

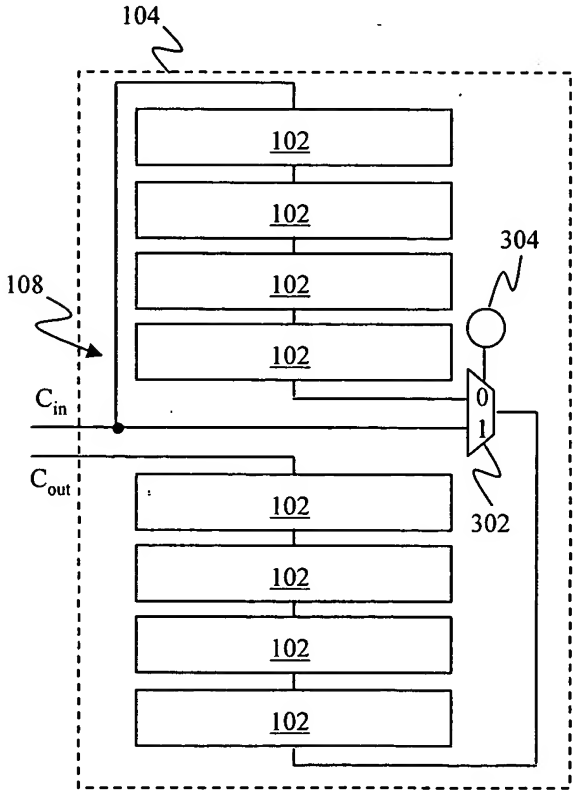
104
102
102
102
102
304
108
C_{in}
0
1
C_{out}
302
102
102
102
102

FIG. 3

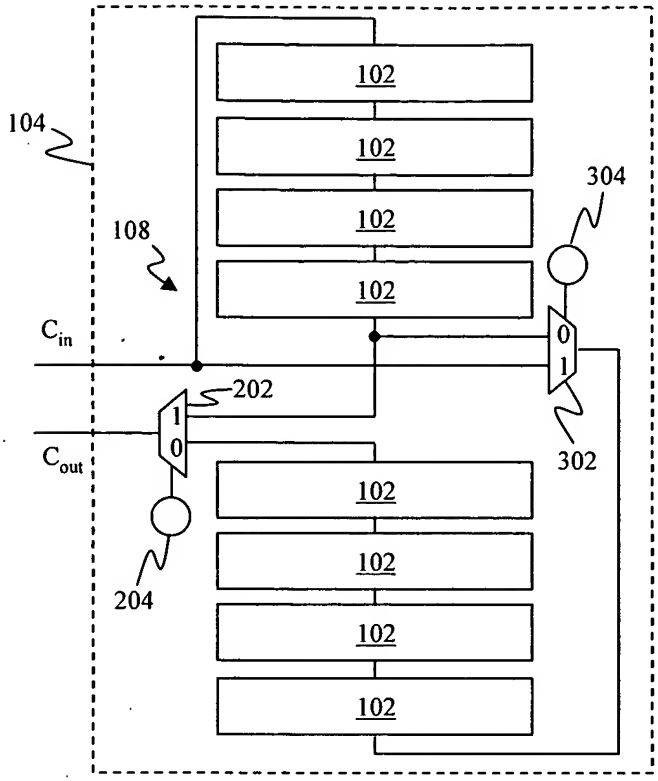
104
102
102
102
102
304
108
C_{in}
0
1
202
1
0
C_{out}
302
102
102
102
102
204

FIG. 4

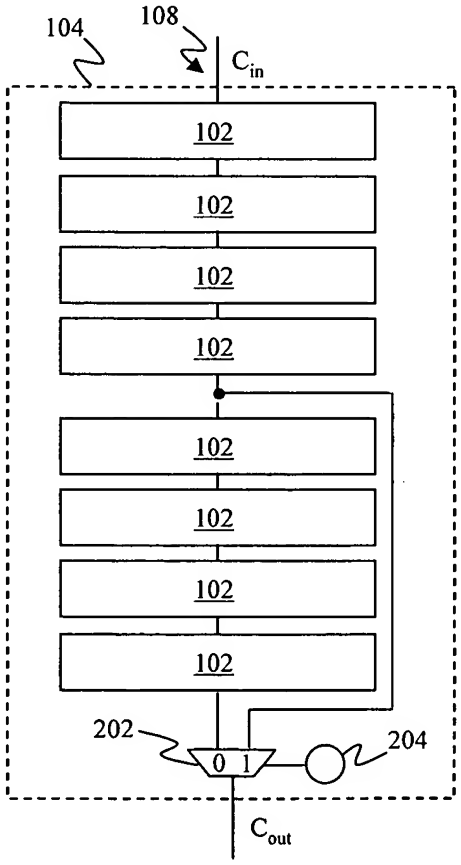
104
108
C_{in}
102
102
102
102
102
102
102
102
202
0 1
204
C_{out}

FIG. 5

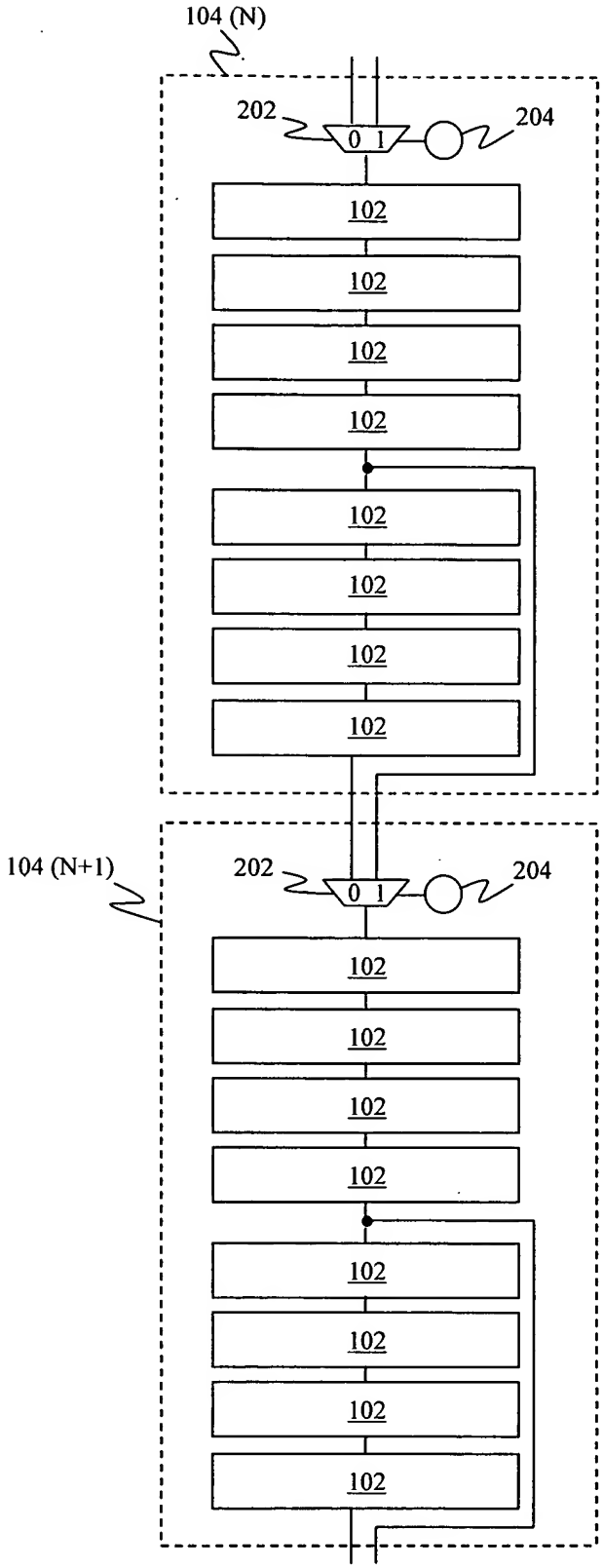
104 (N)
202
0 1
204
102
102
102
102
102
102
102
102
102
104 (N+1)
202
0 1
204
102
102
102
102
102
102
102
102
102

FIG. 6

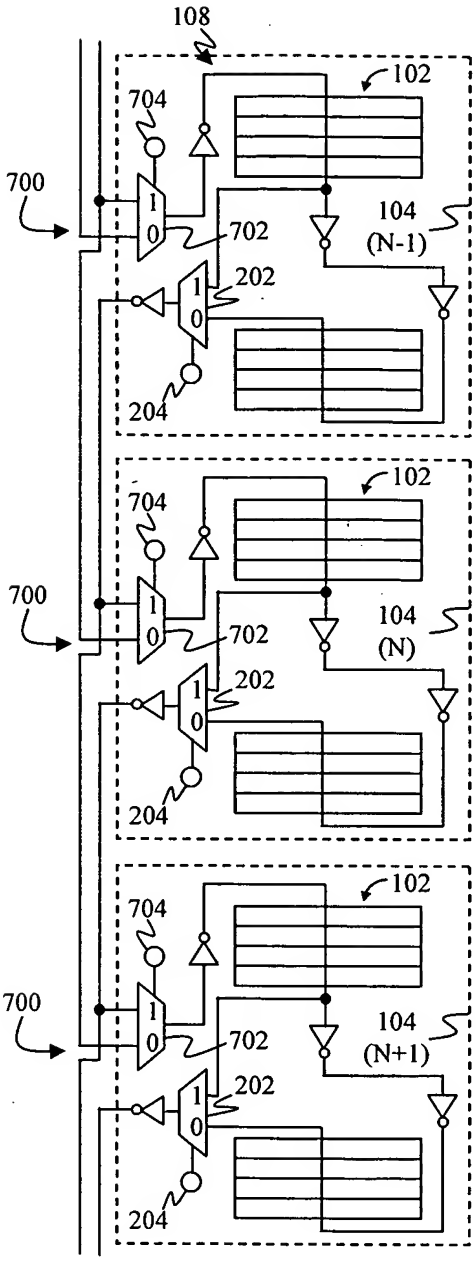
108
102
704
700
1
0
702
104
(N-1)
202
204
102
704
700
1
0
702
104
(N)
202
204
102
704
700
1
0
702
104
(N+1)
202
204

FIG. 7

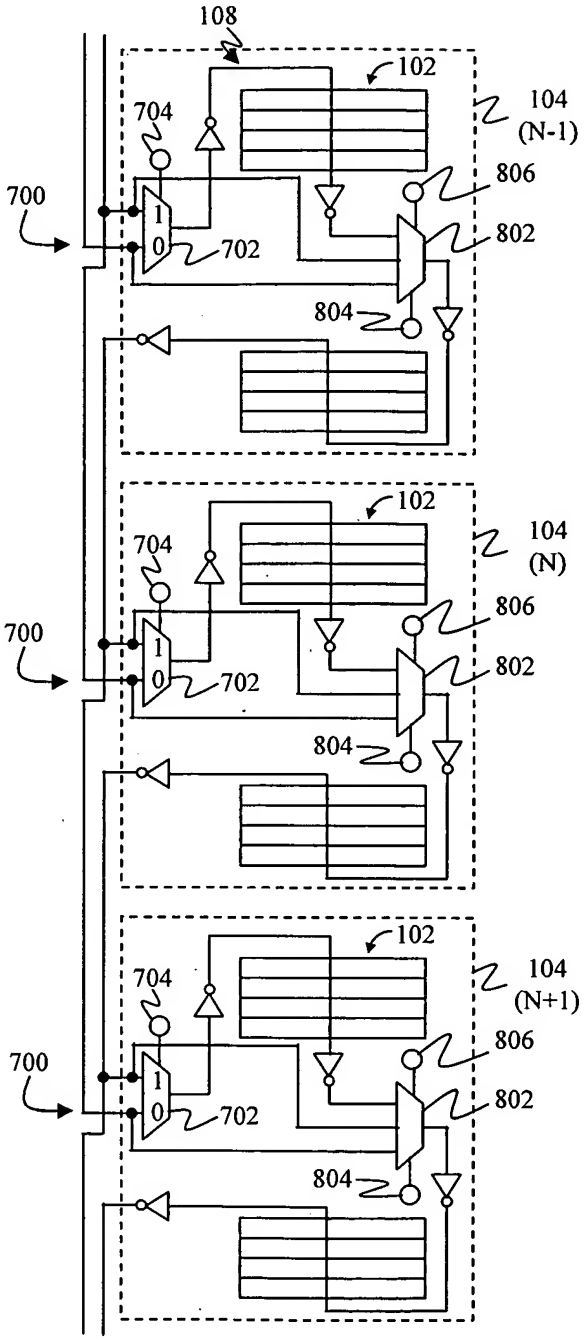
108
102
704
104
(N-1)
700
1
0
702
806
802
804
102
704
104
(N)
700
1
0
702
806
802
804
102
704
104
(N+1)
700
1
0
702
806
802
804

FIG. 8

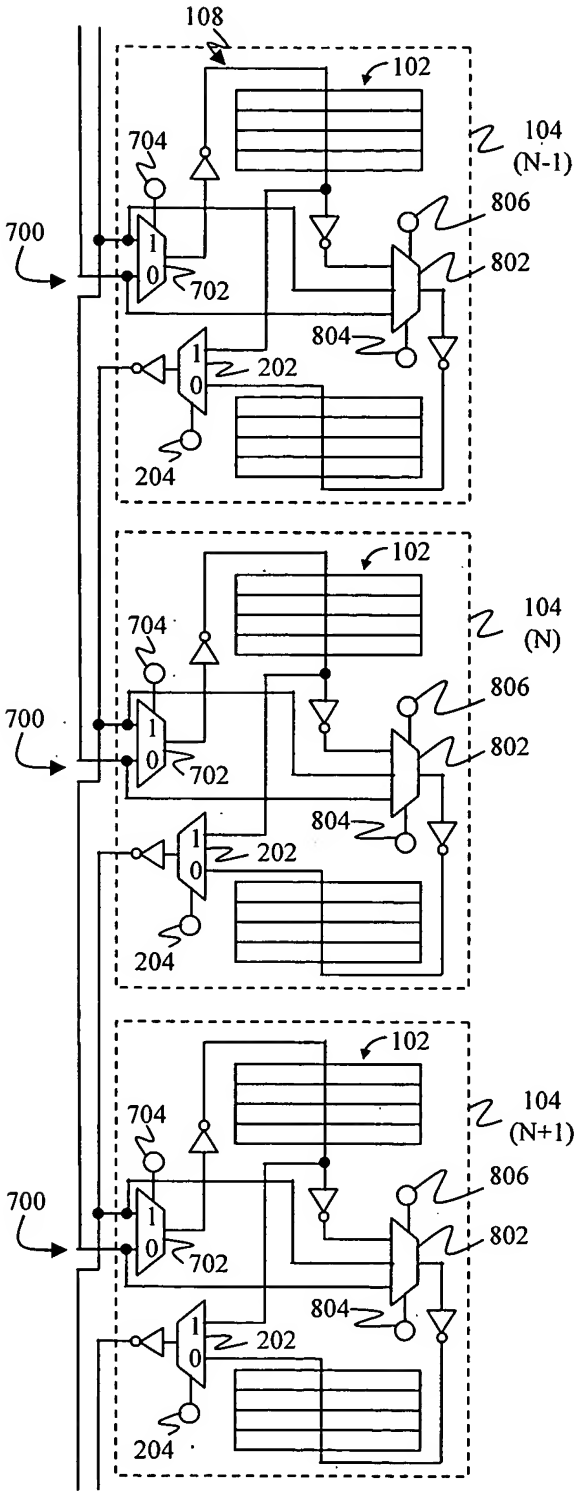
108
102
104
(N-1)
704
806
700
802
702
804
202
204
102
104
(N)
704
806
700
802
702
804
202
204
102
104
(N+1)
704
806
700
802
702
804
202
204

FIG. 9

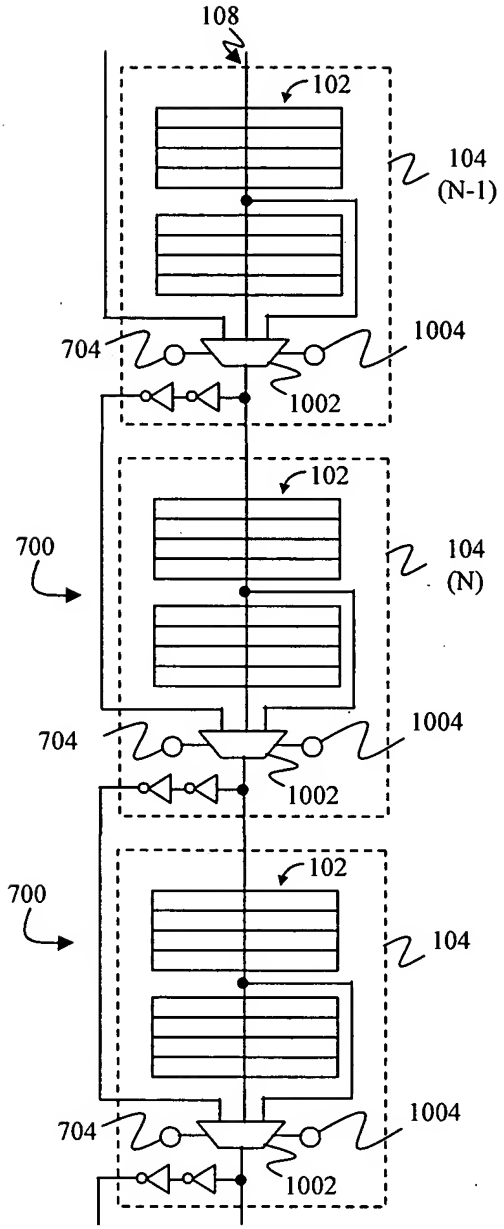
108
102
104
(N-1)
704
1004
1002
102
700
104
(N)
704
1004
1002
102
700
104
704
1004
1002

FIG. 10

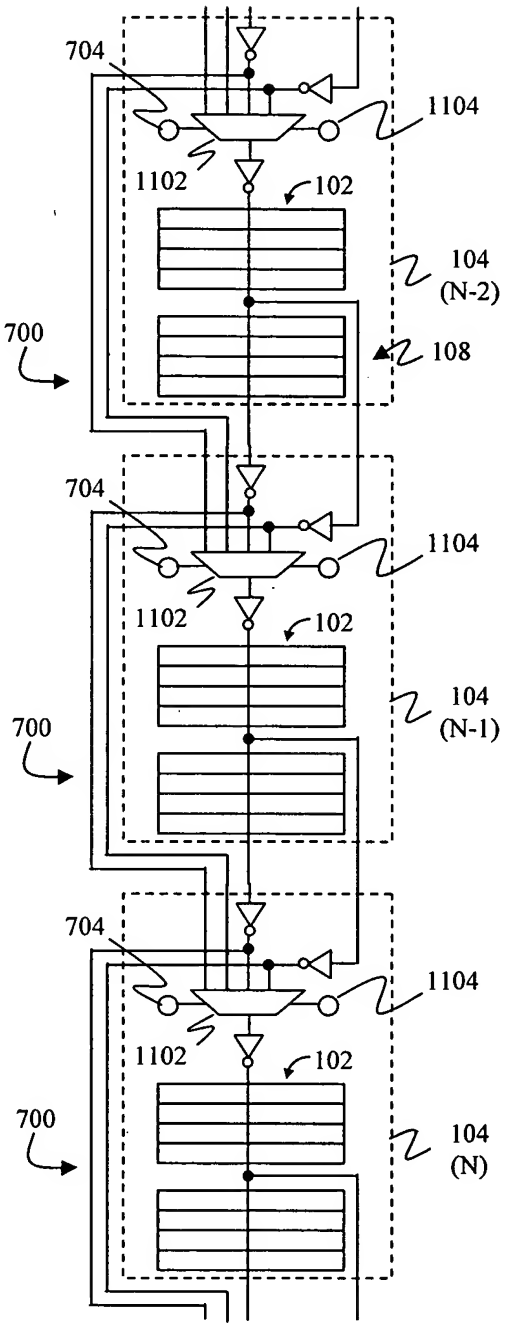
704
1104
1102
102
104
(N-2)
700
108
704
1104
1102
102
104
(N-1)
700
704
1104
1102
102
700
104
(N)

FIG. 11

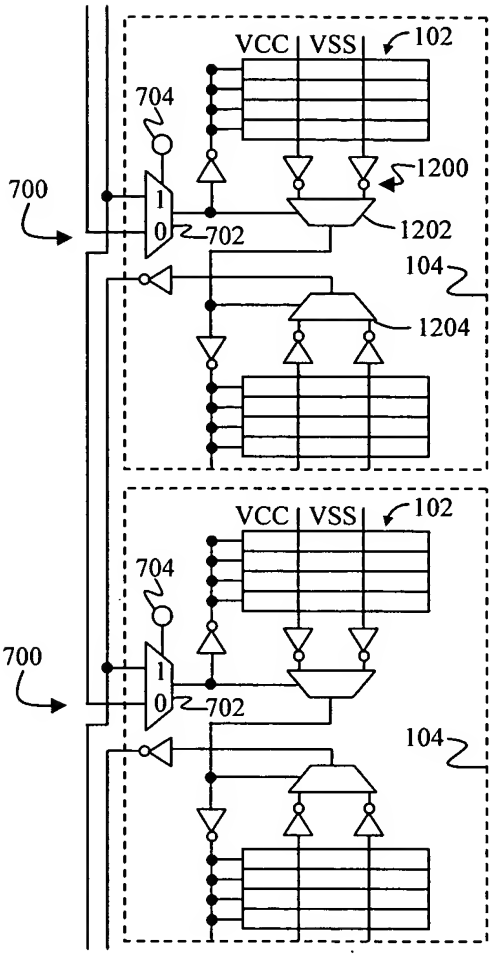
VCC
VSS
102
704
700
1
0
702
1200
1202
104
1204
VCC
VSS
102
704
700
1
0
702
104

FIG. 12

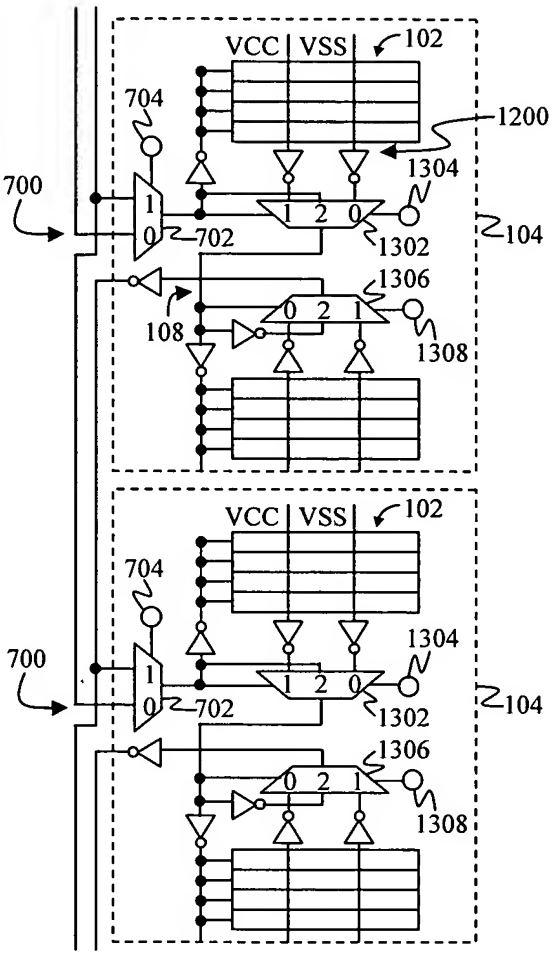
VCC
VSS
102
704
700
1200
1304
1
0
702
1302
104
1306
108
1308
VCC
VSS
102
704
700
1304
1
0
702
1302
104
1306
1308

FIG. 13

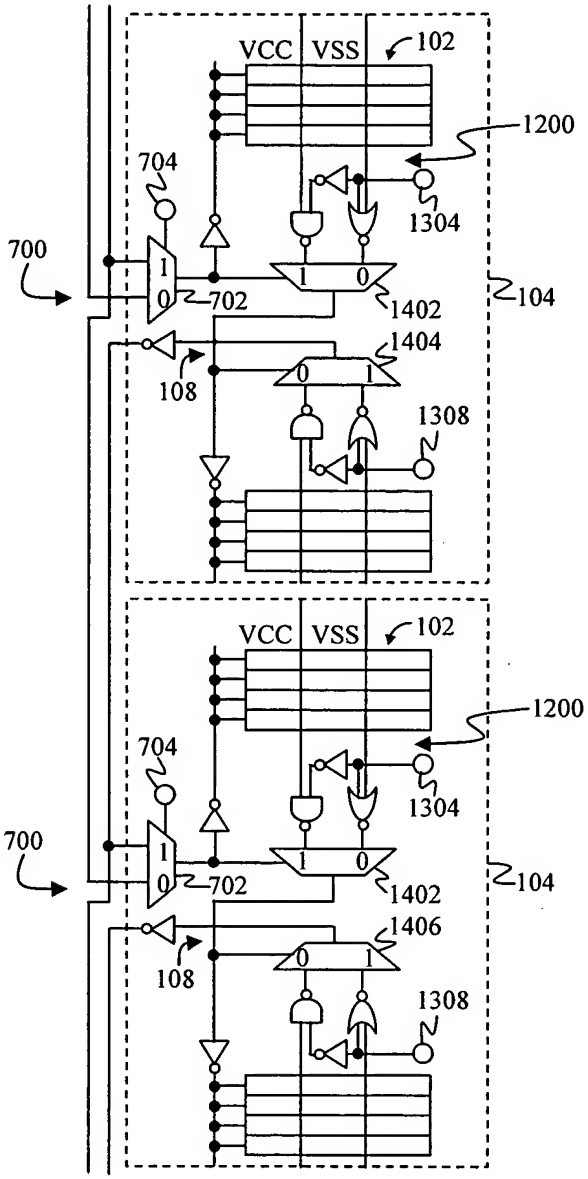
VCC
VSS
102
1200
704
1304
700
1
0
1
0
702
1402
104
1404
0
1
108
1308
VCC
VSS
102
1200
704
1304
700
1
0
1
0
702
1402
104
1406
0
1
108
1308

FIG. 14

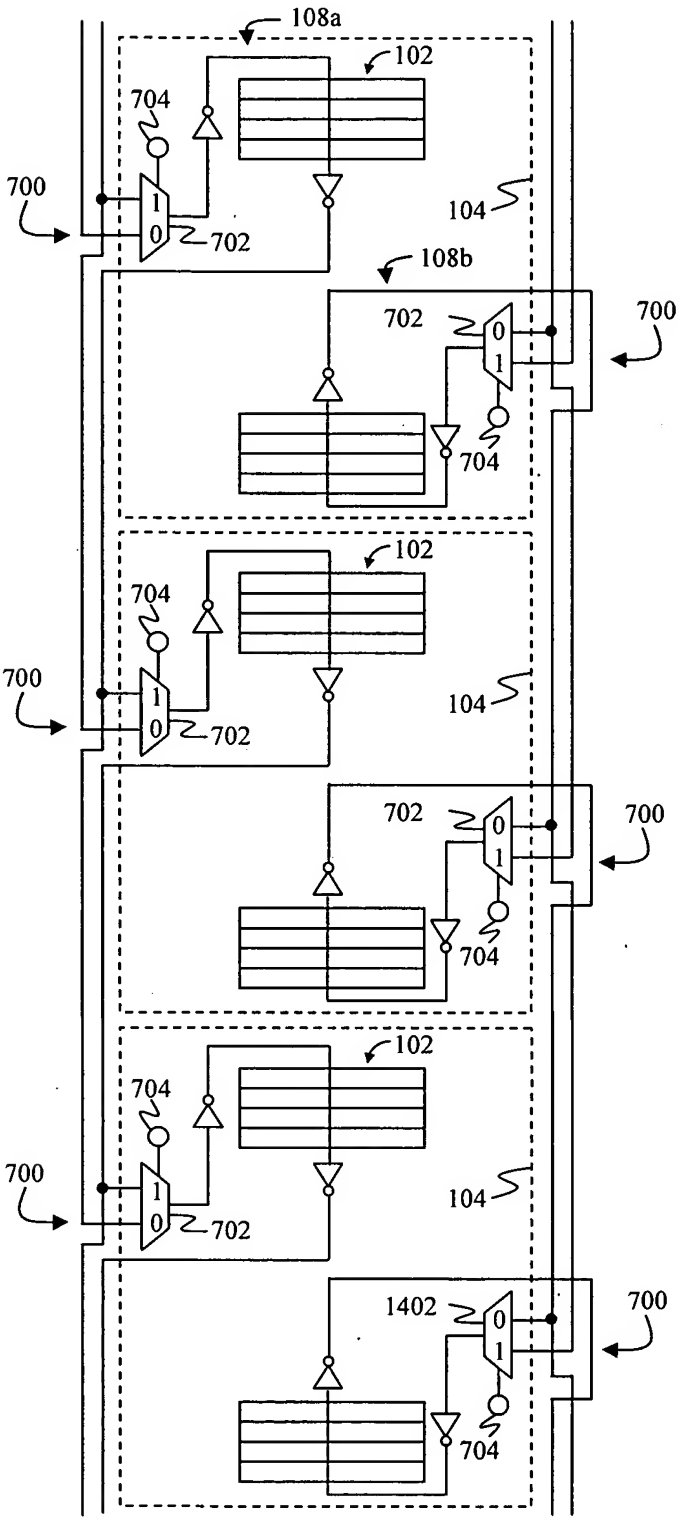
108a
102
704
700
1
0
702
104
108b
702
0
1
700
704
102
704
700
1
0
702
104
702
0
1
700
704
102
704
700
1
0
702
104
1402
0
1
700
704

FIG. 15

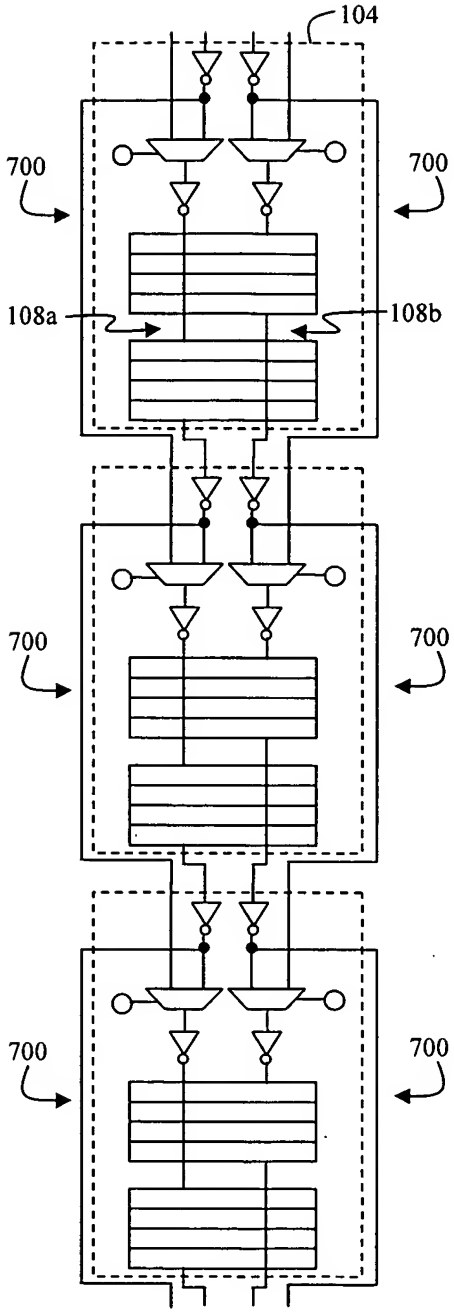
104
700
700
108a
108b
700
700
700
700
700
700

FIG. 16

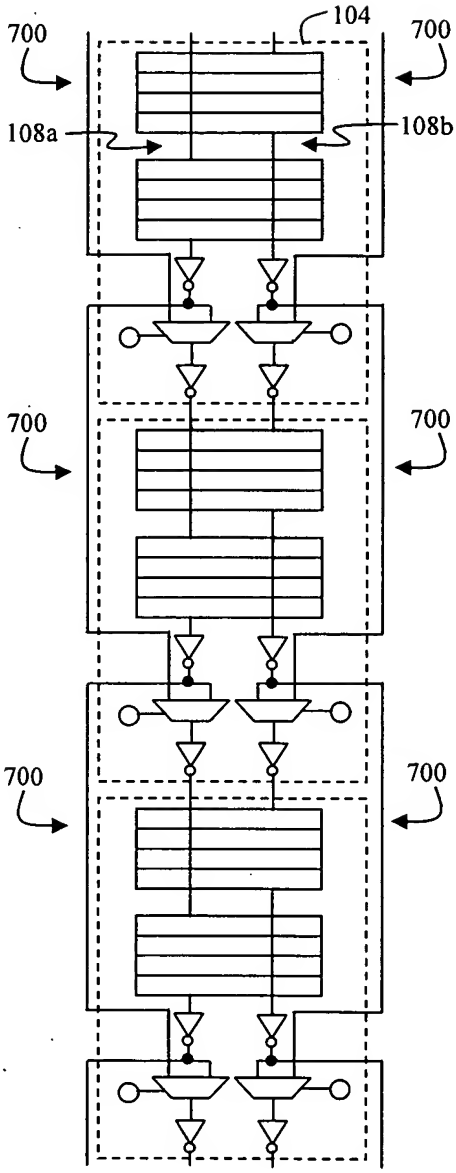
104
700
700
108a
108b
700
700
700
700

FIG. 17

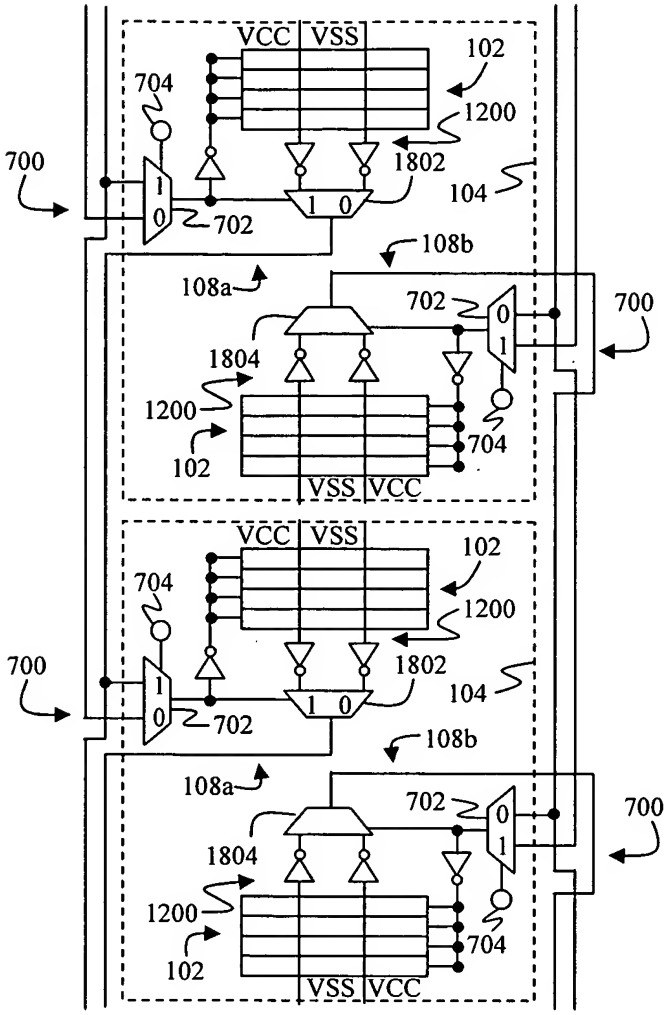

FIG. 18

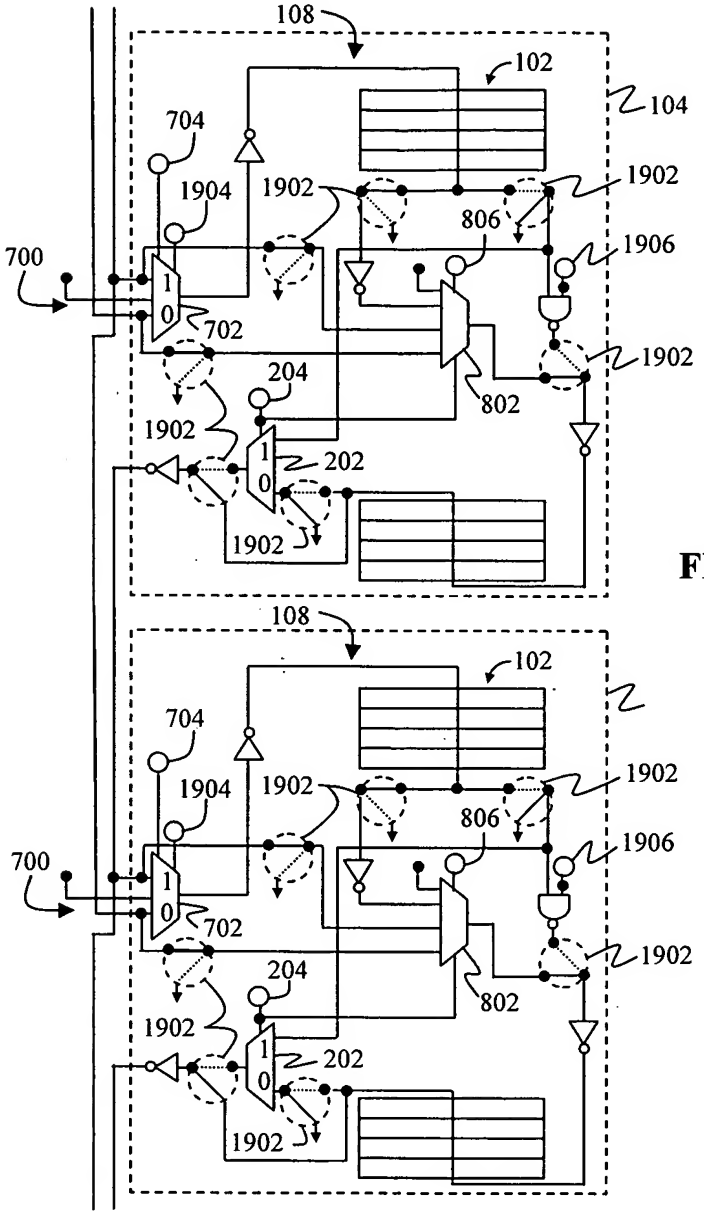
108
102
104
704
1904
1902
1902
806
1906
700
1
0
702
1902
204
802
1902
1
202
0
1902
108
102
704
1904
1902
1902
806
1906
700
1
0
702
1902
204
802
1902
1
202
0
1902

FIG. 19

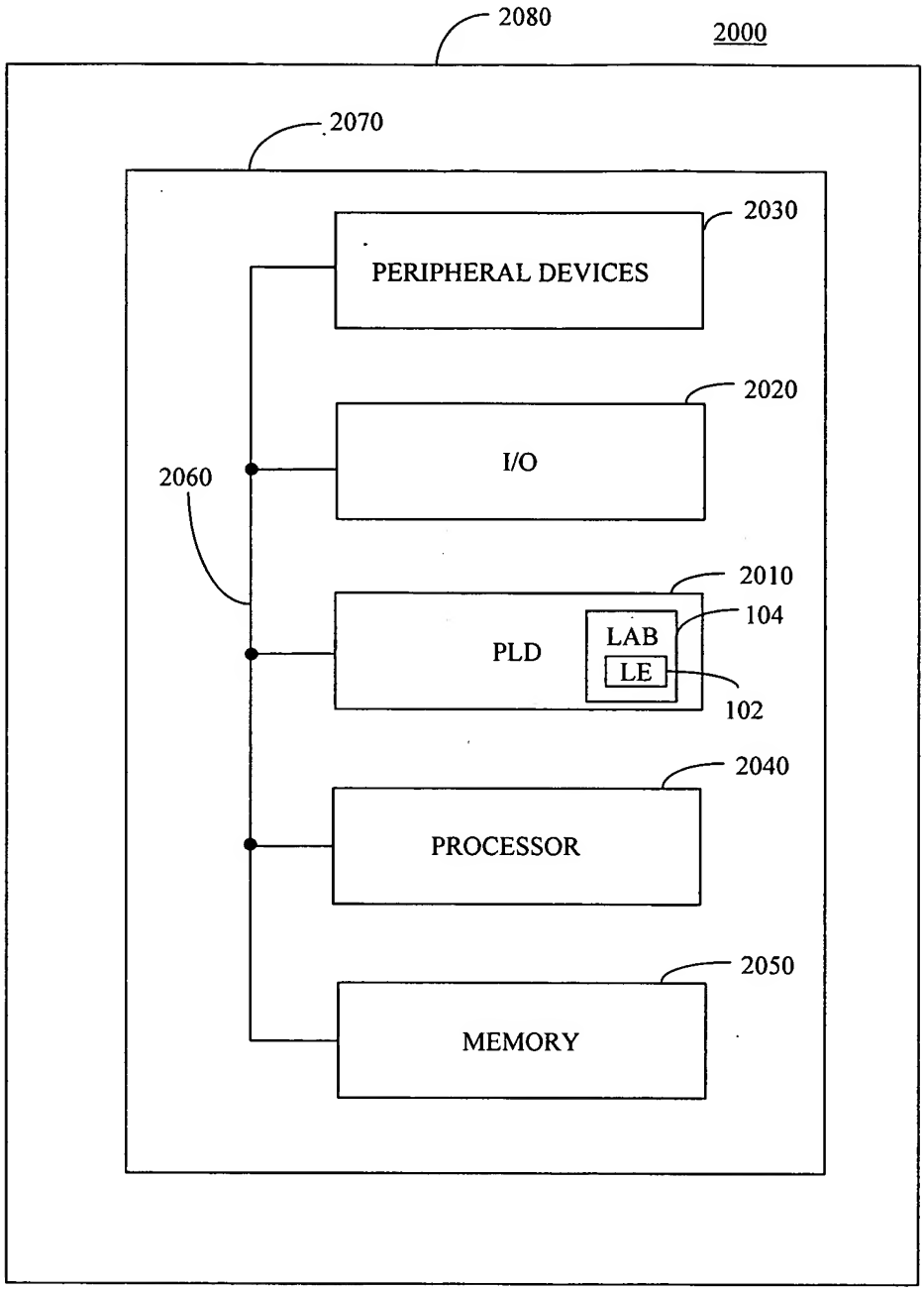
2080
2000
2070
2030
PERIPHERAL DEVICES
2020
I/O
2060
2010
PLD
LAB
LE
104
102
2040
PROCESSOR
2050
MEMORY

FIG. 20